1 kHz to 10 GHz, 64 dB Dynamic Range Dual Log Detector/Controller

Preliminary Technical Data

ADL5519

FEATURES

Wide bandwidth: 1 kHz to 10 GHz
Dual-channel and channel difference output ports
Integrated accurate scaled temperature sensor
64 dB dynamic range
Stability over temperature ±0.5 dB (-40°C to +85°C)
Low noise detector/controller outputs
Pulse response time: 8/10 ns (fall/rise)
Supply operation: 3.0 V to 5.5 V @ 56 mA
Fabricated using high speed SiGe process
Small footprint 5 mm x 5 mm, LFCSP
Operating temperature range –40°C to +125°C

APPLICATIONS

RF Power Amplifier linearization & Gain/Power control
Power monitoring in radio link transmitters
Dual-channel wireless infrastructure radios
Antenna VSWR monitor
RSSI measurement in base stations, WLAN, WiMAX, Radar

GENERAL DESCRIPTION

The ADL5519 is a dual-demodulating logarithmic amplifier. It has the capability of accurately converting an RF input signal to a corresponding decibel-scaled output. The ADL5519 provides accurately scaled, independent, logarithmic outputs of both RF measurement channels. Difference output ports, which measure the difference in power between the two channels, are also available. The on-chip channel matching makes the log-amp channel difference outputs extremely stable with temperature and process variations. The device also includes a useful temperature sensor with an accurately scaled voltage proportional to temperature, specified over the device operating temperature range.

The ADL5519 maintains accurate log conformance for signals of 1 kHz to 8 GHz and provides useful operation to 10 GHz. The input dynamic range is typically 64 dB with linearity better than ±3dB and 50 dB (re: 50 Ω) with error less than ±.5 dB. Response times of 8/10 ns (fall time/rise time) enables RF burst detection to a pulse rate beyond 50 MHz. The device provides unprecedented logarithmic slope and intercept stability vs. ambient temperature conditions. A supply of 3.0 V to 5.5 V is required to power the device. Current consumption is typically 56 mA, and it decreases to less than 1 mA when the device is disabled.

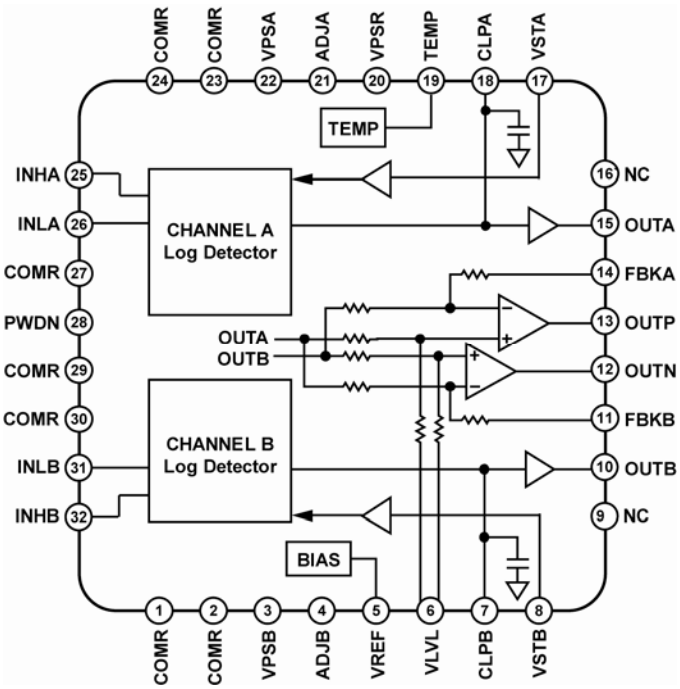

Figure 1. Functional Block Diagram

The device is capable of supplying four log-amp measurements simultaneously. Linear-in-dB measurements are provided at OUTA and OUTB, with conveniently scaled slopes of -22 mV/dB. The log-amp difference between OUTA and OUTB is available as differential or single-ended signals at OUTP and OUTN. An optional voltage applied to VLVL provides a common mode reference level to offset OUTP and OUTN above ground. On-chip wide bandwidth output op amps are used to accommodate flexible configurations that support many system solutions.

The ADL5519 can be easily configured to provide a control voltage to a VGA at any output pin. Since the output can be used for controller applications, special attention has been paid to minimize wideband noise

The ADL5519 is fabricated using a High Speed SiGe bipolar IC process and is available in 5 mm × 5 mm, 32-lead LFCSP package for an operating temperature range of –40°C to +125°C.

Rev. PrC

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SPECIFICATIONS

V_{POS} = 5 V, C_{LPF} = 1000 pF, T_A = 25°C, 52.3 Ω termination resistor at INH[A,B], unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INH[A, B] (Pins 25, 32)				
Specified Frequency Range		0.000001		10	GHz
DC Common-Mode Voltage			V_{POS} – 0.6		V
MEASUREMENT MODE	OUT[A, B] (Pins 15, 10) shorted to VST[A,B] (Pin 17, 8), OUT[P, N] (Pins 13, 12) shorted to FBK[A, B] [Pins 14, 11] respectively, sinusoidal input signal, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = +25°C				
f = 100 MHz	ADJA = ADJB = 0.6V				
Input Impedance			1500||0.33		Ω||pF
±1 dB Dynamic Range	T_A = +25°C		50		dB
	−40°C < T_A < +85°C		46		dB
INH[A,B] Maximum Input Level	±1 dB error		−3		dBm
INH[A,B] Minimum Input Level	±1 dB error		−53		dBm
OUT[A, B, P, N] Slope			−22		mV/dB
OUT[A, B] Intercept			15		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.58		V
Output Voltage - Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.27		V
f = 900 MHz	ADJA = ADJB = 0.55V				
Input Impedance			1500||0.33		Ω||pF
±3 dB Dynamic Range	T_A = +25°C		64		dB
±1 dB Dynamic Range	T_A = +25°C		50		dB
	−40°C < T_A < +85°C		46		dB
INH[A,B] Maximum Input Level	±1 dB error		−3		dB
INH[A,B] Minimum Input Level	±1 dB error		−53		
OUT[A, B, P, N] Slope			−22		dBm
OUT[A, B] Intercept			15		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.58		mV/dB
Output Voltage - Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.27		dBm
f = 1.9 GHz	ADJA = ADJB = 0.5 V				
Input Impedance			950||0.38		Ω||pF
±1 dB Dynamic Range	T_A = +25°C		50		dB
	−40°C < T_A < +85°C		48		dB
INH[A, B] Max Input Level	±1 dB error		−4		dBm
INH[A, B] Min Input Level	±1 dB error		−54		dBm
OUT[A, B, P, N] Slope			−22		mV/dB
OUT[A, B] Intercept			14		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.54		V
Output Voltage – Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.21		V
f = 2.2 GHz	ADJA = ADJB = 0.45V				
Input Impedance			810||0.39		Ω||pF

Parameter	Conditions	Min	Typ	Max	Unit
±1 dB Dynamic Range	T_A = +25°C		50		dB
	−40°C < T_A < +85°C		47		dB
INH[A, B] Maximum Input Level	±1 dB error		−5		dBm
INH[A, B] Minimum Input Level	±1 dB error		−55		dBm
OUT[A, B, P, N] Slope			−22		mV/dB
OUT[A, B] Intercept			14		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.53		V
Output Voltage - Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.20		V
f = 3.6 GHz	ADJA = ADJB = 0.375V				
Input Impedance			300||0.33		Ω||pF
±1 dB Dynamic Range	T_A = +25°C		42		dB
	−40°C < T_A < +85°C		40		dB
INH[A, B] Maximum Input Level	±1 dB error		−6		dBm
INH[A, B] Minimum Input Level	±1 dB error		−48		dBm
OUT[A, B, P, N] Slope			−22		mV/dB
OUT[A, B] Intercept			11		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.47		V
Output Voltage - Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.16		V
f = 5.8 GHz	ADJA = ADJB = 0.65V				
Input Impedance			110||0.05		Ω||pF
±1 dB Dynamic Range	T_A = +25°C		50		dB
	−40°C < T_A < +85°C		48		dB
INH[A, B] Maximum Input Level	±1 dB error		−4		dBm
INH[A, B] Minimum Input Level	±1 dB error		−54		dBm
OUT[A, B, P, N] Slope			−22		mV/dB
OUT[A, B] Intercept			16		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.59		V
Output Voltage - Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.27		V
f = 8 GHz	ADJA = ADJB = 0.95V				
Input Impedance			28||0.79		Ω||pF
±1 dB Dynamic Range	T_A = +25°C		44		dB
	−40°C < T_A < +85°C		TBD		dB
INH[A, B] Maximum Input Level	±1 dB error		−2		dBm
INH[A, B] Minimum Input Level	±1 dB error		−46		dBm
OUT[A, B, P, N] Slope			−22		mV/dB
OUT[A, B] Intercept			21		dBm
Output Voltage - High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		0.7		V
Output Voltage - Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		1.39		V
OUTPUT INTERFACE	OUT[A, B] (Pins 15, 10), OUT[P, N] (Pins 13, 12)				
OUT[A, B] Voltage Range Min	VST[A, B] = 1.7V; RFIN = open		0.3		V
OUT[A, B] Voltage Range Max	VST[A, B] = 0V; RFIN = open		V_{POS} – 0.3		V
OUT[P, N] Voltage Range Min	FBK[A, B] = ? RFIN = open RL ≥ 240Ω to ground		0.09		V
OUT[P, N] Voltage Range Max	FBK[A, B] = 0V RFIN = open RL ≥ 240Ω to ground		Vs – 0.15		V
Source/Sink Current	Output held at 1V to 1% change		2.2		mA
Small Signal Bandwidth	RFIN = −10 dBm, from CLP[A,B] to OUT[A,B]		100		MHz
Output Noise	RF Input = 2.2 GHz, −10 dBm, f_{NOISE} = 100 kHz, $C_{LP[A,B]}$ =		20		

Parameter	Conditions	Min	Typ	Max	Unit
	open				nV/√Hz
Fall Time	Input level = no signal to –10 dBm, 90% to 10%, $C_{LP[A,B]}$ = 8 pF		18		ns
Fall Time	Input level = no signal to –10 dBm, 90% to 10%, $C_{LP[A,B]}$ = open;		6		ns
Rise Time	Input level = –10 dBm to no signal, 10% to 90%, $C_{LP[A, B]}$ = 8 pF		20		ns
Rise Time	Input level = –10 dBm to no signal, 10% to 90%, $C_{LP[A,B]}$ = open,		10		ns
Video (or Envelope) Bandwidth			50		MHz
SETPOINT INTERFACE	VST[A, B] (Pins 8, 17)				
Nominal Input Range	INH[A,B] = 0 dBm, measurement mode		0.35		V
	INH[A,B] = –50 dBm, measurement mode		1.40		V
Logarithmic Scale Factor			–45		dB/V
Input Resistance	INH[A,B] = –20 dBm, controller mode, VST[A,B] = 1 V		40		kΩ
DIFFERENCE LEVEL ADJUST	VLVL (Pin 6)				
Voltage Range	OUT[P, N] = FBK[A, B]	0		V_{POS}	V
OUT[P, N] Voltage Range	OUT[P, N] = FBK[A, B]	.3		V_{POS} -.3	V
Input Impedance			1		KΩ
TEMPERATURE COMPENSATION	ADJ[A, B] (Pins 21, 4)				
Input Voltage Range			0 – 1.2		V
Input Resistance	ADJ[A, B] = 0.9 V, sourcing 50 µA		> 10		MΩ
VOLTAGE REFERENCE	VREF (Pin 5)				
Output Voltage	INH[A,B]=TBD		1.15		V
Temperature Sensitivity	–40°C < T_A < +85°C		TBD		mV/°C
Current Limit Source/Sink			3/3		mA
TEMPERATURE REFERENCE	TEMP (Pin 19)				
Output Voltage	T_A = 25°C		1.3		V
Temperature Sensitivity	–40°C < T_A < +125°C		4.5		mV/°C
Current Limit Source/Sink	T_A = 25°C, 1% Change		5/40		mA
POWER-DOWN INTERFACE	PWDN (Pin 28), ADJ[A,B] (Pins 21, 4)				
Logic Level to Enable	Logic LO Enables			1	V
Logic Level to Disable	Logic HI Disables	V_{POS}-0.7			V
Input Current	Logic HI PWDN = ADJ[A, B] = 5V		95		µA
	Logic LO PWDN = ADJ[A, B] = 0V			100	µA
POWER INTERFACE	VPS[A, B, R] (Pins 22, 3, 20)				
Supply Voltage		3.0		5.5	V
Quiescent Current			56		mA
vs. Temperature	–40°C ≤ T_A ≤ +125°C		60		µA/°C
Disable Current	ADJ[A,B] = PWDN = VPOS		< 1		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: VPSA, VPSB, VPSR	5.7 V
V_{SET} Voltage: VSTA, VSTB	0 to V_{POS}
Input Power (Single-Ended, Re: 50 Ω) INHA, INLA, INHB, INLB	12 dBm
Internal Power Dissipation	
θ_{JA}	55°C/W
Maximum Junction Temperature	165°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

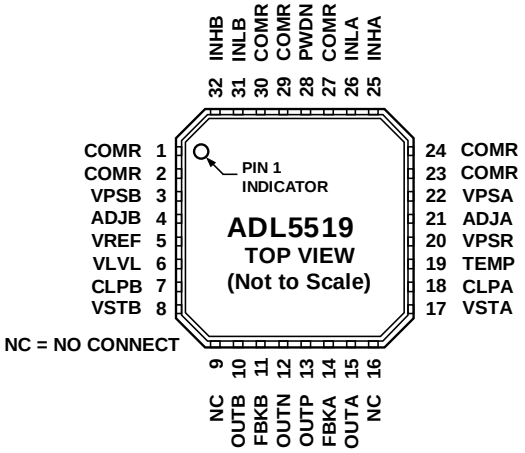


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

PIN	Name	Description
1	COMR	Connect via low impedance to common
2	COMR	Connect via low impedance to common
3	VPSB	Positive Supply for Channel B. Apply 3.0V to 5.5V supply voltage.
4	ADJB	Dual function pin. Temperature adjust Pin for Channel B and Power down interface for OUTB.
5	VREF	1.15V voltage reference
6	VLVL	DC common mode adjust for difference output
7	CLPB	Loop filter pin for Channel B
8	VSTB	Setpoint Control input for Channel B
9	NC	No Connect
10	OUTB	Output voltage for Channel B
11	FBKB	Difference op-amp feedback pin for OUTN opamp
12	OUTN	Difference output (OUTB - OUTA + VLVL)
13	OUTP	Difference output (OUTA - OUTB + VLVL)
14	FBKA	Difference op-amp feedback pin for OUTP opamp
15	OUTA	Output voltage for Channel A
16	NC	No Connect
17	VSTA	Setpoint Control input for Channel A
18	CLPA	Loop filter pin for Channel A
19	TEMP	Temp Sensor output (1.3V with 4.5mV/°C slope)
20	VPSR	Positive supply for difference outputs & temperature sensor. Apply 3.0V to 5.5V supply voltage.
21	ADJA	Dual function pin. Temperature adjust Pin for Channel A and Power down interface for OUTA.
22	VPSA	Positive Supply for Channel A. Apply 3.0V to 5.5V supply voltage.
23	COMR	Connect via low impedance to common
24	COMR	Connect via low impedance to common
25	INHA	AC coupled RF input for Channel A
26	INLA	AC coupled RF common for Channel A
27	COMR	Connect via low impedance to common
28	PWDN	Power down for difference output and Temp Sensor
29	COMR	Connect via low impedance to common
30	COMR	Connect via low impedance to common
31	INLB	AC coupled RF common for Channel B
32	INHB	AC coupled RF input for Channel B
	Paddle	Internally connected to COMR

THEORY OF OPERATION

The ADL5519 is a dual-channel 6-stage demodulating logarithmic amplifier, specifically designed for use in RF measurement and power control applications at frequencies up to 10 GHz. Sharing much of its design with the AD8317 logarithmic detector/controller, each channel of the ADL5519 maintains tight slope and intercept variability vs. temperature over a 50 dB range. The complete circuit block diagram is shown in Figure 3.

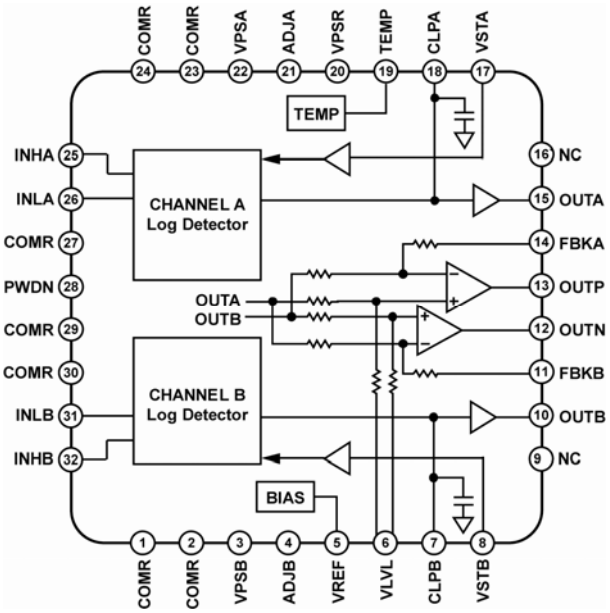


Figure 3. Block Diagram

Each measurement channel is a fully differential design (that can be run single ended) using a proprietary, High Speed SiGe process, extending high frequency performance. Figure 4 shows the basic diagram of the ADL5519's channel A signal path, the functionality is identical for channel B.

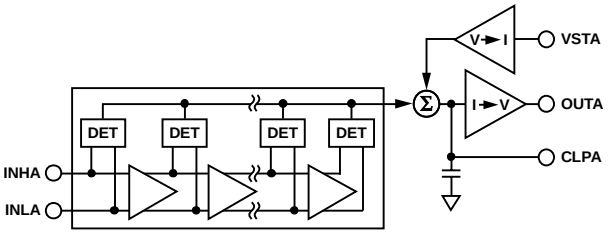


Figure 4. Single Channel Block Diagram

The maximum input with ±1 dB log-conformance error is typically 0 dBm (re: 50 Ω). The noise spectral density referred to the input is 1.15 nV/√Hz, which is equivalent to a voltage of 118 μV rms in a 10.5 GHz bandwidth or a noise power of −66 dBm (re: 50 Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low end accuracy of the ADL5519 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise. The common pin, COMR, provides a quality low impedance connection to the printed circuit board (PCB) ground. The package paddle, which is internally connected to the COMR pin, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by six cascaded gain stages. (For a more comprehensive explanation of the logarithm approximation, please refer to the AD8307 data sheet, available at www.analog.com.) The cells have a nominal voltage gain of 9 dB each and a 3 dB bandwidth of 10.5 GHz. Using precision biasing, the gain is stabilized over temperature and supply variations. The overall dc gain is high, due to the cascaded nature of the gain stages. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each of the gain stages, a square-law detector cell is used to rectify the signal.

The RF signal voltages are converted to a fluctuating differential current having an average value that increases with signal level. Along with the six gain stages and detector cells, an additional detector is included at the input of each measurement channel, providing a 50 dB dynamic range in total. After the detector currents are summed and filtered, the following function is formed at the summing node:

$$I_D \times \log_{10}(V_{IN}/V_{INTERCEPT})$$

where:

I_D is the internally set detector current. V_{IN} is the input signal voltage. $V_{INTERCEPT}$ is the intercept voltage (that is, when $V_{IN} = V_{INTERCEPT}$, the output voltage would be 0 V, if it were capable of going to 0 V).

USING THE ADL5519

BASIC CONNECTIONS

ADL5519 is specified for operation up to 10 GHz; as a result, low impedance supply pins with adequate isolation between functions are essential. A power supply voltage of between 3.0 V and 5.5 V should be applied to VPSA, VPSB, and VPSR. Power supply decoupling capacitors of 100 pF and 0.1 µF should be connected close to these power supply pins.

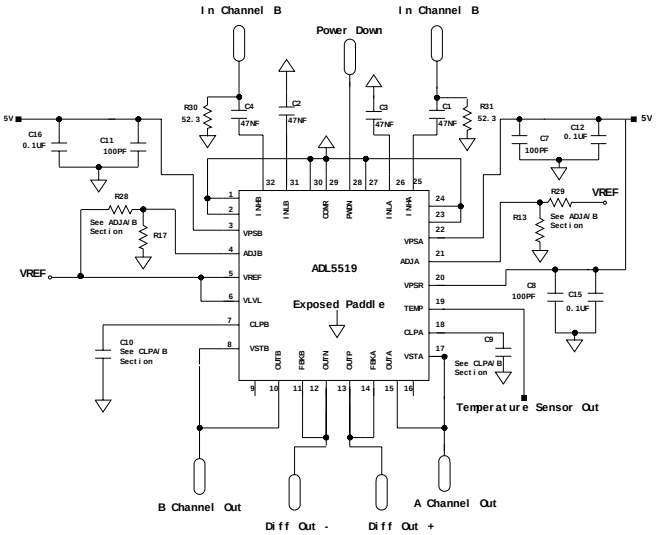


Figure 5. Basic Connections

The paddle of the LFCSP_VD package is internally connected to COMR. For optimum thermal and electrical performance, the paddle should be soldered to a low impedance ground plane.

INPUT SIGNAL COUPLING

The RF inputs (INHA and INHB) are single-ended and must be ac-coupled. INLA and INLB (input common) should be ac-coupled to ground. Suggested coupling capacitors are 47nF ceramic 0402-style capacitors for input frequencies of 1 MHz to 10 GHz. The coupling capacitors should be mounted close to the INH[A,B] and INL[A,B] pins. The coupling capacitor values can be increased to lower the input stage's high-pass cutoff frequency. The high-pass corner is set by the input coupling capacitors and the internal 10pF high-pass capacitor. The dc voltage on INH[A,B] and INL[A,B] is about one diode voltage drop below the supply voltage.

While the input can be reactively matched, in general this is not necessary. An external 52.3 Ω shunt resistor, connected on the signal side of the input coupling capacitors (and as close to the ADL5519 as possible, as shown in Figure 5), combines with the relatively high input impedance to give an adequate broadband 50 Ω match.

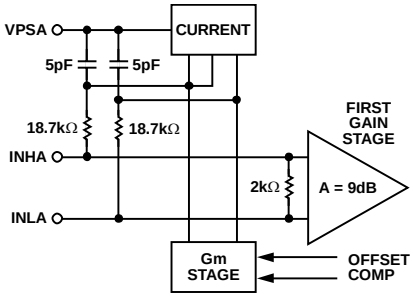


Figure 6. Single Channel Input Interface

The coupling time constant, $50 \times C_C/2$, forms a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(2\pi \times 50 \times C_C)$, where C1 = C2 = C_C. Using the typical value of 47nF, this high pass corner will be ~68 kHz. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low-pass filter should be added at the input for similar reasons. This should generally be placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

TEMPERATURE SENSOR INTERFACE

The ADL5519 provides a temperature sensor output capable of driving about >2 mA. The Temperature-scaling factor of the output voltage is ~ 4.48 mV/°C. The typical absolute voltage at 27°C is about 1.3V.

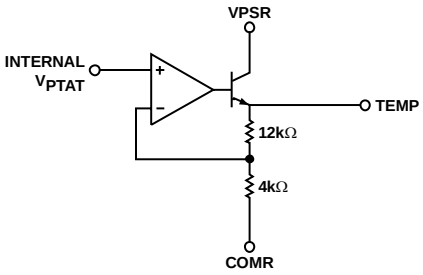


Figure 7. TEMP Interface Simplified Schematic

POWER-DOWN INTERFACE

The operating and stand-by currents for the ADL5519 at 27°C are approximately 65 mA and 1 mA, respectively. The PWDN and ADJ[A,B] pins are connected to the base of and NPN transistor to force a power down condition. Typically, when PWDN is pulled >VPOS-0.6 V, the ADL5519 is powered down from 65mA to <1mA. When powered on, the output reaches to within 0.1 dB of its steady-state value in about 1.6 µs; the reference voltage is available to full accuracy in a much shorter time. This wake-up response time varies depending on the input coupling network and the capacitance at pins CLP[A, B].

The individual log channels can be disabled by installing a 0Ω pull up resistor from ADJ[A,B] to VPS[A,B].

SETPOINT INTERFACE, VST[A, B]

The V_{SET} input drives the high impedance (40 kΩ) input of an internal op amp. The V_{SET} voltage appears across the internal 1.5 kΩ resistor to generate a current I_{SET}. When a portion of V_{OUT} is applied to VSET, the feedback loop forces

$$-I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET}.$$

If $V_{SET} = V_{OUT}/2x$, then $I_{SET} = V_{OUT}/(2x \times 1.5\ k\Omega)$.

The result is

$$V_{OUT} = (-I_D \times 1.5\ k\Omega \times 2x) \times \log_{10}(V_{IN}/V_{INTERCEPT})$$

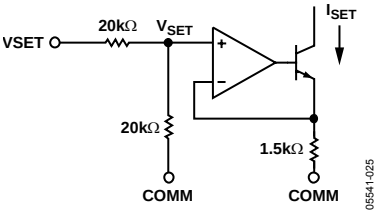


Figure 8. VST[A, B] Interface Simplified Schematic

The slope is given by $-I_D \times 2x \times 1.5\ k\Omega = -22\ mV/dB \times x$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, then x = 2. The slope is set to −880 V/decade or −44 mV/dB.

OUTPUT INTERFACE, OUT[A, B]

The OUT[A,B] pins are driven by a Push-Pull output stage.. The rise time of the output is limited mainly by the slew on CLP[A,B]. The fall time is an RC-limited slew given by the load capacitance and the pull-down resistance at OUT[A,B]. There is an internal pull-down resistor of 1.6 kΩ. A resistive load at OUT[A,B] can be placed in parallel with the internal pull-down resistor to reduce the discharge time.

OUT[A, B] can source 2.2 mA.

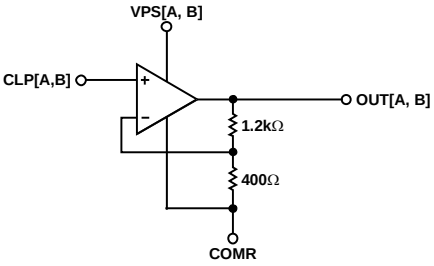


Figure 9. OUT[A, B] Interface Simplified Schematic

DIFFERENCE OUTPUT, OUT[P, N]

The ADL5519 incorporates two operational amplifiers with rail-to-rail output capability to provide a channel difference output.

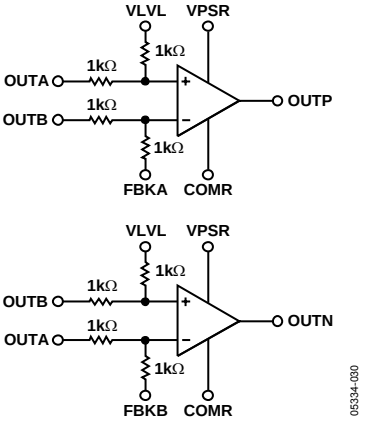


Figure 10. OUT[P, N] Interface Simplified Schematic

As in the case of the output drivers for OUT[A, B], the output stages have the capability of driving 2.2 mA. OUTA and OUTB are internally connected through 1 kΩ resistors to the inputs of each op amp. The pin VLVL is connected to the positive terminal of both op amps through 1kΩ resistors to provide level shifting. The negative feedback terminal is also made available through a 1kΩ resistor. The input impedance of VLVL is 1kΩ and FBK[A, B] is 2 kΩ. See Figure 11 for the block diagram of these pins.

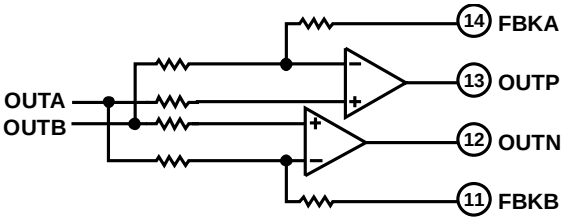


Figure 11. Op Amp Connections (All Resistors are 1 kΩ ± 20%)

If OUTP is connected to FBKA, then OUTP is given as

$$OUTP = OUTA - OUTB + VLVL \quad (9)$$

If OUTN is connected to FBKB, then OUTN is given as

$$OUTN = OUTB - OUTA + VLVL \quad (10)$$

In this configuration, all four measurements, OUT[A, B, P, N], are made available simultaneously. A differential output can be taken from OUTP − OUTN, and VLVL can be used to adjust the common-mode level for an differential ADC connection.

MEASUREMENT MODE

The device is placed in measurement mode by connecting OUT[A,B] to VST[A,B], respectively. The ADL5519 has an offset voltage, a negative slope, and a $V_{OUT[A,B]}$ measurement intercept at the high end of its input signal range.

The output voltage vs. input signal voltage of the ADL5519 is linear-in-dB over a multidecade range. The equation for this function is of the form

$$V_{OUT} = X \times V_{SLOPE/DEC} \times \log_{10}(V_{IN}/V_{INTERCEPT}) = \quad (1)$$

$$X \times V_{SLOPE/dB} \times 20 \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (2)$$

where:

X is the feedback factor in $V_{SET} = V_{OUT}/X$. $V_{SLOPE/DEC}$ is nominally −440 mV/decade or −22 mV/dB. $V_{INTERCEPT}$ is the x-axis intercept of the linear-in-dB portion of the V_{OUT} vs. V_{IN} curve. $V_{INTERCEPT}$ is +2 dBV for a sinusoidal input signal.

An offset voltage, V_{OFFSET}, of 0.35 V is internally added to the detector signal, so that the minimum value for V_{OUT} is $X \times V_{OFFSET}$. So for X = 1, minimum V_{OUT} is 0.35 V.

The slope is very stable vs. process and temperature variation. When base-10 logarithms are used, $V_{SLOPE/DECADE}$ represents the volts/decade. A decade corresponds to 20 dB; $V_{SLOPE/DECADE}/20 = V_{SLOPE/dB}$ represents the slope in volts/dB.

As noted in Equation 1 and Equation 2, the V_{OUT} voltage has a *negative* slope. This is also the correct slope polarity to control the gain of many VGA's in a negative feedback configuration. Because both the slope and intercept vary slightly with frequency, it is recommended to refer to the Specifications section for application-specific values for slope and intercept.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_0, must be known to convert voltages to their corresponding power levels. The following equations are used to perform this conversion:

$$P(\text{dBm}) = 10 \times \log_{10}(V_{rms}^2/(Z_0 \times 1\text{ mW})) \quad (3)$$

$$P(\text{dBV}) = 20 \times \log_{10}(V_{rms}/1\ V_{rms}) \quad (4)$$

$$P(\text{dBm}) = P(\text{dBV}) - 10 \times \log_{10}(Z_0 \times 1\text{ mW}/1\ V_{rms}^2) \quad (5)$$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal expressed in terms of dBm (decibels referred to 1 mW), in a 50 Ω system is

$$P_{INTERCEPT}(\text{dBm}) = P_{INTERCEPT}\ (\text{dBV}) - 10 \times \log_{10}(Z_0 \times 1\text{ mW}/1\ V_{rms}^2) = \quad (6)$$

$$+2\text{ dBV} - 10 \times \log_{10}(50 \times 10^{-3}) = +15\text{ dBm}$$

For a square wave input signal in a 200 Ω system,

$$P_{INTERCEPT} = -1\text{ dBV} - 10 \times \log_{10}[(200\ \Omega \times 1\text{ mW}/1V_{rms}^2)] = +6\text{ dBm}$$

Further information on the intercept variation dependence upon waveform can be found in the AD8313 and AD8307 data sheets.

As the input signal to Channel A and Channel B are swept over their nominal input dynamic range of +10 dBm to −50 dBm, the output swings from 0.5 V to 1.75 V. The voltages OUTA and OUTB are also internally applied to a difference amplifier with a gain of two and applied to OUTP and OUTN. So as the dB difference between INA and INB ranges from approximately −30 dB to +30 dB, the difference voltage on OUTP and OUTN swings from 0.5 V to 1.75 V. Input differences larger than ±30 dB can be measured as long as the absolute input level at INA and INB are within their nominal ranges of +10 dBm to −50 dBm. However, measurement of large differences between INA and INB are affected by on-chip signal leakage. The common-mode level of OUTP and OUTN is set by the voltage applied to VLVL. These output can be easily biased up to a common-mode voltage of 2.5 V by connecting VREF to VLVL. As the gain range is swept, OUTP swings from approximately 0.5 V to Vcc-0.3V and OUTN swings from Vcc-0.3V to 0.5 V.

CONTROLLER MODE

In addition to being a measurement device, the ADL5519 can also be configured to measure and control signal levels. The ADL5519 has two controller modes. Each of the two log detectors can be separately configured to set and control the output power level of a variable gain amplifier (VGA) or variable voltage attenuator (VVA). Alternatively, the two log detectors can be configured to measure and control the *gain* of an amplifier or signal chain.

The channel difference outputs can be used for controlling a feedback loop to the ADL5519's RF inputs. A capacitor connected between FBKA and OUTP (or FBKB and OUTN for the opposite slope) forms an integrator, keeping in mind that the on-chip 1 kΩ feedback resistor forms a zero. (The value of the on-chip resistors can vary as much as ±20% with manufac-turing process variation.) If Channel A is driven and Channel B has a feedback loop from OUTP through a PA, then OUTP integrates to a voltage value such that

$$OUTB = (OUTA + VLVL)/2 \quad (11)$$

The output value from OUTN may or may not be useful. It is given by

$$OUTN = 0\text{ V} \quad (12)$$

For VLVL < OUTA/3,

Otherwise,

$$OUTN = (3 \times VLVL - OUTA)/2 \quad (13)$$

If VLVL is connected to OUTA, then OUTB is forced to equal OUTA through the feedback loop. This flexibility provides the user with the capability to measure one channel operating at a given power level and frequency while forcing the other channel to a desired power level at another frequency. ADJA and ADJB should be set to different voltage levels to reduce the temperature drift of the output measurement. The temperature drift will be statistical sum of the drift from Channel A and Channel B. As stated before, VLVL can be used to force the slaved channel to

operate at a different power than the other channel. If the two channels are forced to operate at different power levels, then some static offset occurs due to voltage drops across metal wiring in the IC.

If an inversion is necessary in the feedback loop, OUTN can be used as the integrator by placing a capacitor between OUTN and OUTP. This changes the output equation for OUTB and OUTP to

$$OUTB = 2 \times OUTA - VLVL \quad (14)$$

For VLVL < OUTA/2,

$$OUTN = 0 \text{ V} \quad (15)$$

Otherwise,

$$OUTN = 2 \times VLVL - OUTA \quad (16)$$

The previous equations are valid when Channel A is driven and Channel B is slaved through a feedback loop. When Channel B is driven and Channel A is slaved, the above equations can be altered by changing OUTB to OUTA and OUTN to OUTP.

TEMPERATURE COMPENSATION

The ADL5519 has a highly stable measurement output with respect to temperature. However, when the RF inputs exceed a frequency of 600 MHz, the output temperature drift must be compensated for applying a voltage at ADJ[A, B] for optimal performance. With appropriate values, a temperature drift error of typically ±0.5 dB or better over the entire rated temperature range can be achieved.

Proprietary techniques were used to compensate for the temperature drift. The absolute value of compensation varies with frequency and circuit board material.

Compensating the device for temperature drift using ADJ[A, B] allows for great flexibility. If the user requires minimum temperature drift at a given input power or subset of the dynamic range, the ADJ[A, B] voltage can be swept while monitoring OUT[A, B] over temperature. The proper value for ADJ[A, B] is the voltage where the output voltage is the same for all temperatures at a particular power level and frequency.

The ADJ[A, B] pins have a high input impedance. The input can be conveniently driven from an attenuated value of VREF using a resistor divider, if desired. The ADJ[A, B] pins can also be used to disable the ADL5519, as detailed in the Power-Down Interface Section

Figure 12 shows a simplified schematic representation of the ADJ[A, B] interface.

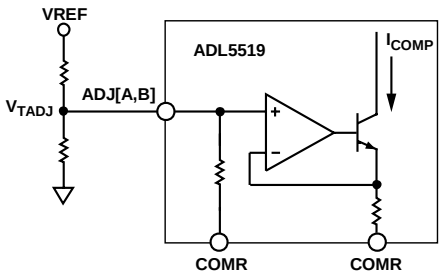


Figure 12. ADJ[A, B] Interface Simplified Schematic

DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. The equation for output voltage can be written as

$$V_{OUT} = Slope \times (P_{IN} - Intercept)$$

Where *Slope* is the change in output voltage divided by the change in power (dB), and *Intercept* is the calculated power at which the output voltage would be 0 V. (Note that *Intercept* is a theoretical value; the output voltage can never achieve 0 V).

The simplest way to perform this calibration is by applying two known signal levels to the ADL5519's input and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear-in-dB operating range of the device (see the Specifications section for more details).

Calculation of the slope and intercept is done using the equations:

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2})$$

$$Intercept = P_{IN1} - (V_{OUT1}/Slope)$$

Once slope and intercept have been calculated, an equation can be written that will allow calculation of the input power based on the output voltage of the detector.

$$P_{IN}\,(unknown) = (V_{OUT1(measured)}/Slope) + Intercept$$

The log conformance error of the calculated power is given by

$$Error\ (\text{dB}) = (V_{OUT(\text{MEASURED})} - V_{OUT(IDEAL)})/Slope$$

ALTERING THE SLOPE

None of the changes to operating conditions discussed so far affect the logarithmic slope, V_{SLOPE}, in Equation 7. The slope can readily be altered by controlling the fraction of OUT[A, B] that is fed back to the setpoint interface at the VST[A, B] pin. When the full signal from OUT[A, B] is applied to VST[A, B], the slope assumes its nominal value of -22 mV/dB. It can be increased by including a voltage divider between these pins, as shown in Figure 13. Moderately low resistance values should be used to minimize scaling errors due to the approximately 40 kΩ input resistance at the VST[A, B] pin. Keep in mind that this resistor string also loads the output, and it eventually reduces

the load-driving capabilities if very low values are used. Equation 17 can be used to calculate the resistor values.

$$R1 = R2' (S_D/-22 - 1) \quad (17)$$

where:
S_D is the desired slope, expressed in mV/dB.
$R2'$ is the value of R2 in parallel with 40 kΩ.

For example, using R1 = 1.65 kΩ and R2 = 1.69 kΩ ($R2'$ = 1.62 kΩ), the nominal slope is increased to -44 mV/dB.

Operating at a high slope is useful when it is desired to measure a particular section of the input range in greater detail.

When the slope is raised by some factor, the loop capacitor, CLP[A, B], should be raised by the same factor to ensure stability and to preserve a chosen averaging time. The slope can be lowered by placing a voltage divider after the output pin, following standard practice.

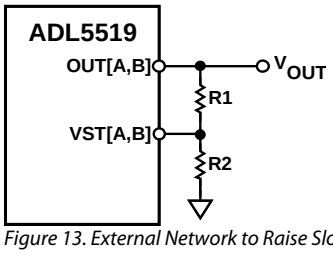


Figure 13. External Network to Raise Slope

OUTPUT FILTERING

Accurate power detection for signals with RF bursts is achieved when the ADL5519 is able to respond quickly to the change in RF power. For applications in which maximum video bandwidth and, consequently, fast rise time are desired, it is essential that the CLP[A,B] pin be left unconnected and free of any stray capacitance.

The nominal output video bandwidth of 50 MHz can be reduced by connecting a ground-referenced capacitor (C_{FLT}) to the CLPF pin, as shown in Figure 14. This is generally done to reduce output ripple (at twice the input frequency for a symmetric input waveform such as sinusoidal signals).

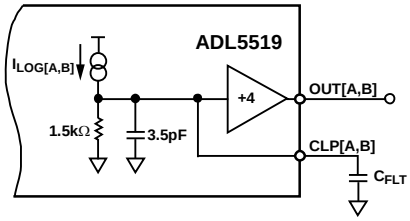


Figure 14. Lowering the Post demodulation Bandwidth

C_{FLT} is selected using the following equation:

$$C_{FLT} = \frac{1}{(\pi \times 1.5\ \text{k}\Omega \times \textit{Video Bandwidth})} - 3.5\ \text{pF} \quad (10)$$

The video bandwidth should typically be set to a frequency equal to about one-tenth the minimum input frequency. This ensures that the output ripple of the demodulated log output, which is at twice the input frequency, is well filtered.

EVALUATION BOARD

Table 4. Evaluation Board (Rev. A) Configuration Options

Component	Function	Default Conditions
VPOS, VPSB, VPSR	**Supply Connections** VPOS, VPSB, VPSR are routed to the same power supply plane on the evaluation board	3V-5V
GND1, GND2, GND3	**Ground Connections** GND1, GND2, GND3 are internally connected together.	Power Supply Common
R30, R31, C1, C2, C3, C4	**Input Interface** The 52.3 Ω resistor in positions R30 and R31 combine with the ADL5519's internal input impedance to give a broadband input impedance of about 50 Ω. Capacitors C1, C2, C3, and C4 are dc-blocking capacitors. A reactive impedance match can be implemented by replacing R31[R30] with an inductor and C1[C3] and C2[C4] with appropriately valued capacitors.	R30 = 52.3 Ω (Size 0402) C1 = 47 nF (Size 0402) C2 = 47 nF (Size 0402) R31 = 52.3 Ω (Size 0402) C3 = 47 nF (Size 0402) C4 = 47 nF (Size 0402)
R14	**Temperature Sensor Interface** Temperature sensor output voltage is available at the test point labeled TEMP.	R14 = 0 Ω (Size 0603)
R13, R17, R18, R19, R27, R28, R29	**Temperature Compensation Interface** A voltage source at ADJ[A, B] pins can be used to optimize the temperature performance for various input frequencies. The pads for R27/R28 or R27/R29 can be used for voltage dividers from the VREF node to set the ADJ[A, B] voltages at different frequencies. The individual log channels can be disabled by installing 0Ω resistors in positions R18 and R19	R13 = open (size 0603) R17 = open (size 0603) R18 = 0 Ω (size 0603) R19 = 0 Ω (size 0603) R27 = 0 Ω (size 0603) R28 = open (size 0603) R29 = open (size 0603)
R8, R12, R15, R16, R20, R21, R22, R23, C13, C14	**OUTA/OUTB Interface—Measurement Mode** In measurement mode, a portion of the output voltage is fed back to Pin VSTA[VSTB] via R8[R12]. The magnitude of the slope of the OUTA[OUTB] output voltage response can be increased by reducing the portion of V_{OUTA} [V_{OUTB}]that is fed back to VSTA[VSTB]. R20[R21} can be used as a back-terminating resistor or as part of a single-pole, low-pass filter.	R8 = 0 Ω (Size 0603) R12 = 0 Ω (Size 0603) R15 = open (Size 0603) R16 = open (Size 0603) R20 = 0 Ω (Size 0603) R21 = 0 Ω (Size 0603) R22 = open (Size 0603) R23 = open (Size 0603) C13 = open (Size 0603) C14 = open (Size 0603)
R8, R12, R22, R23	**OUTA/OUTB Interface—Controller Mode** In this mode, R8[R12] must be open. In controller mode, the ADL5519 can control the gain of an external component. A setpoint voltage is applied to Pin VSTA[VSTB], the value of which corresponds to the desired RF input signal level applied to the corresponding ADL5519 RF input. A sample of the RF output signal from this variable-gain component is selected, typically via a directional coupler, and applied to ADL5519 RF input. The voltage at Pin OUTA[OUTB] is applied to the gain control of the variable gain element. A control voltage is applied to Pin VSTA[VSTB]. The magnitude of the control voltage can optionally be attenuated via the voltage divider comprising R8[R12] and R22[R23], or a capacitor can be installed in position R22[R23] to form a low-pass filter along with R8[R12].	R8 = open (Size 0603) R12 = open (Size 0603) R22 = open (Size 0603) R23 = open (Size 0603)

R3, R4, R11, C7, C8 C11, C12, C15, C16	**Power Supply Decoupling.** The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the ADL5519 and a 0.1 µF capacitor placed nearer to each power supply input pin. Small valued resistors can be used for R3 and R4 to increase the filtering of the power supply.	R3 = 0 Ω (Size 0603) R4 = 0 Ω (Size 0603) R11 = 0 Ω (Size 0603) C7 = 100 pF (Size 0603) C8 = 100 pF (Size 0603) C11 = 100 pF (Size 0603) C12 = 0.1 µF (Size 0603) C15 = 0.1 µF (Size 0603) C16 = 0.1 µF (Size 0603)
R1, R2, R9, R10	**Output Interface – Difference**	R1 = 0 Ω (Size 0603) R2 = 0 Ω (Size 0603) R9 = 0 Ω (Size 0603) R10 = 0 Ω (Size 0603)
C9, C10	**Filter Capacitor** The low-pass corner frequency of the circuit that drives Pin OUTA[OUTB] can be lowered by placing a capacitor between CLPA[CLPB] and ground. Increasing this capacitor increases the overall rise/fall time of the ADL5519 for pulsed input signals. See the Output Filtering section for more details.	C9 = 100 pF (Size 0603) C10 = 100 pF (Size 0603)

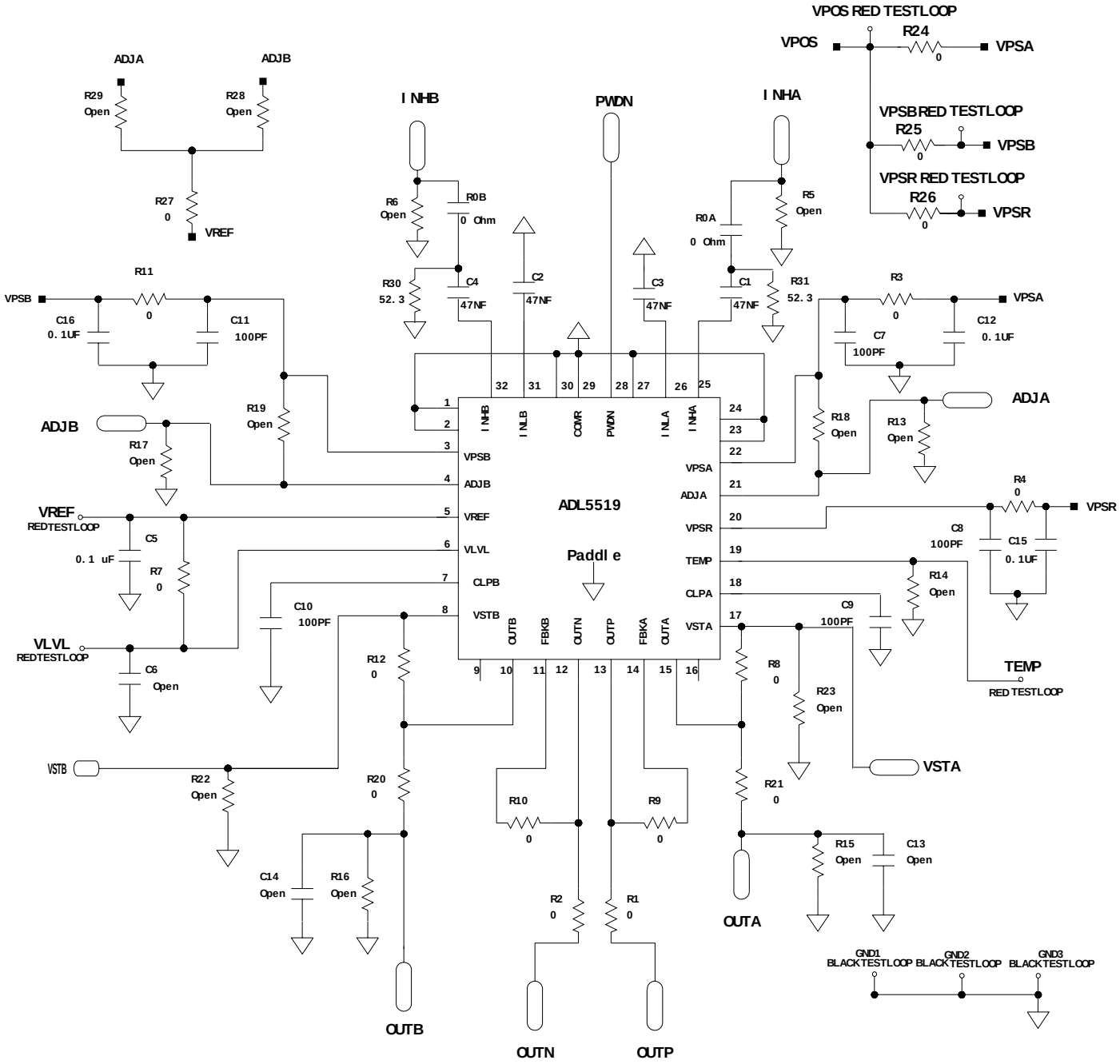


Figure 15. Evaluation Board Schematic

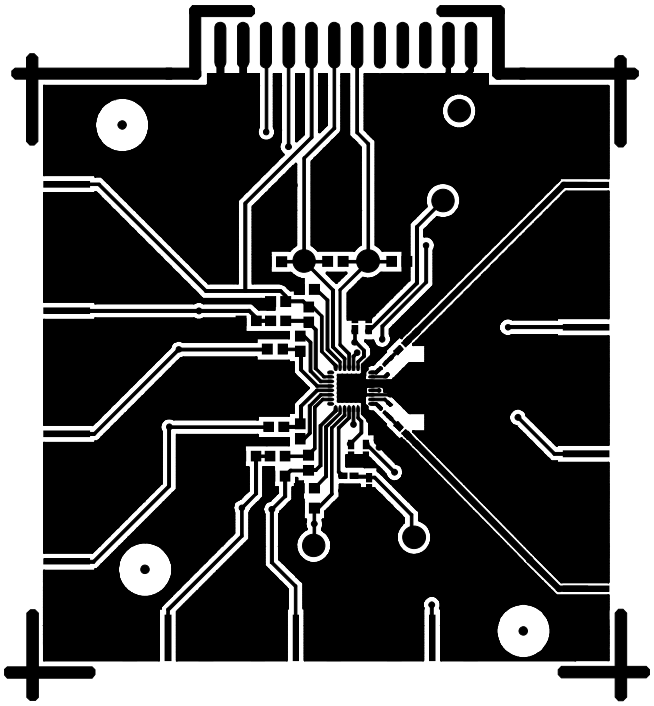


Figure 16. Top Side Layout

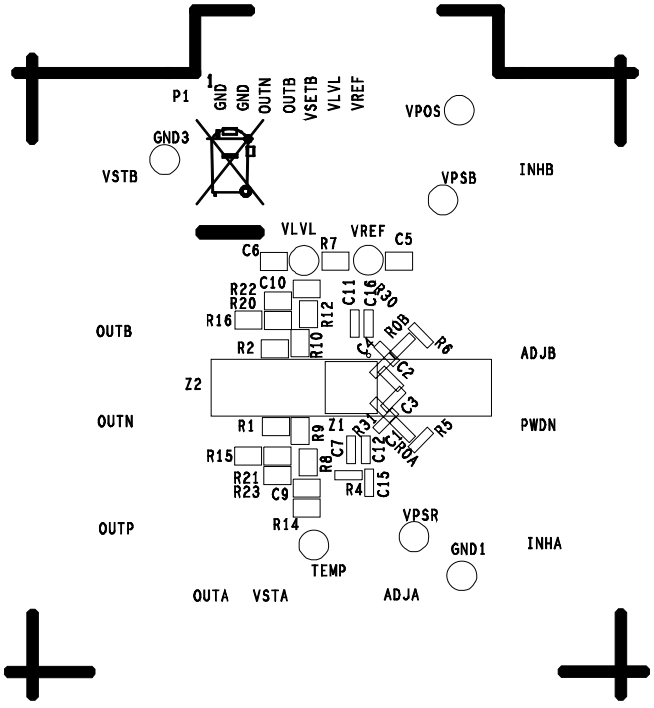


Figure 17. Top Side Silkscreen

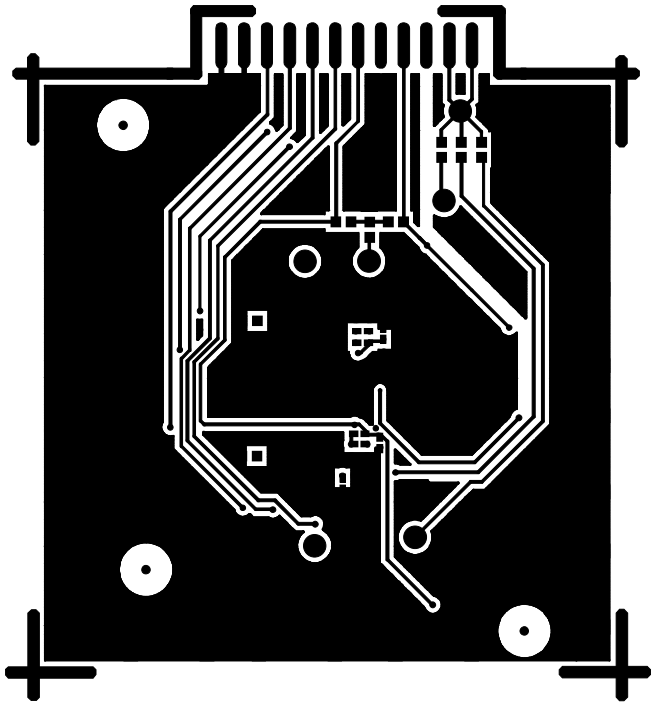


Figure 18: Bottom Side Layout

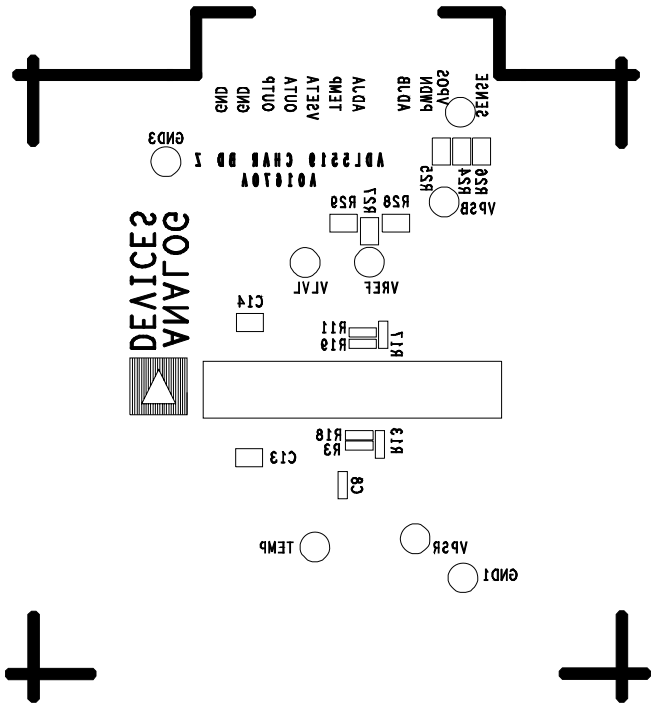
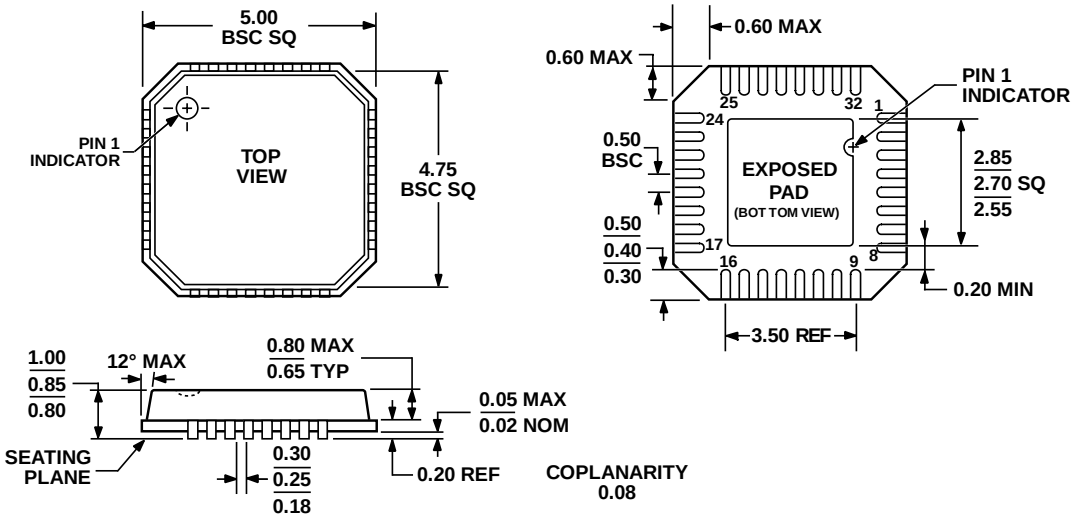


Figure 19: Bottom Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 20. 32-Lead Lead Frame Chip Scale Package [LFCSP_VD]
5 mm x 5 mm Body, Very Thin, Dual Lead
(CP-32-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Option	Branding
ADL5519ACPZ-R7[1]	–40°C to +125°C	32-Lead LFCSP_VD	CP-32-8	TBD
ADL5519ACPZ-R2[1]	–40°C to +125°C	32-Lead LFCSP_VD	CP-32-8	TBD
ADL5519ACPZ-WP[1, 2]	–40°C to +125°C	32-Lead LFCSP_VD	CP-32-8	TBD
ADL5519-EVALZ[1]		Evaluation Board		

[1] Z = Pb-free part.
[2] WP = waffle pack.